

Description

The XPX300N80RD uses advanced trench technology and design to provide excellent $R_{DS(ON)}$ with low gate charge. It can be used in a wide variety of applications.

General Features

- High density cell design for ultra low R_{dson}
- Fully characterized avalanche voltage and current
- Good stability and uniformity with high E_{AS}
- Excellent package for good heat dissipation
- Special process technology for high ESD capability

Application

- Power switching application
- Hard switched and high frequency circuits
- Uninterruptible power supply

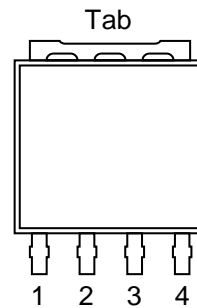


$V_{DS} = 80V, I_D = 300A$

$R_{DS(ON)} = 1.3m\Omega$ (typ) @ $V_{GS} = 10V$

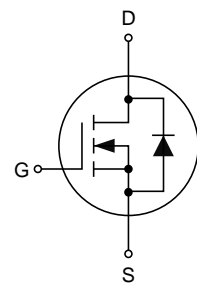
$R_{DS(ON)} = 1.9m\Omega$ (typ) @ $V_{GS} = 4.5V$

Simplified Outline



**Top View
LPAK 5x6**

Symbol



Package Marking and Ordering Information

Device Marking	Device	Device Package	Reel Size	Tape width	Quantity
XPX300N08RD	XPX300N08RD	DFN5X6-8L	-	-	-

Absolute Maximum Ratings ($T_C = 25^\circ C$ unless otherwise noted)

Parameter	Symbol	Limit	Unit
Drain-Source Voltage	V_{DS}	80	V
Gate-Source Voltage	V_{GS}	± 20	V
Drain Current-Continuous	I_D	300	A
Drain Current-Continuous($T_C = 100^\circ C$)	$I_D(100^\circ C)$	235	A
Pulsed Drain Current	I_{DM}	1200	A
Maximum Power Dissipation	P_D	378	W
Derating factor		0.4	W/ $^\circ C$
Operating Junction and Storage Temperature Range	T_J, T_{STG}	-55 To 150	$^\circ C$
Thermal Resistance, Junction-to-Case ^(Note 2)	$R_{\theta JC}$	0.8	$^\circ C/W$

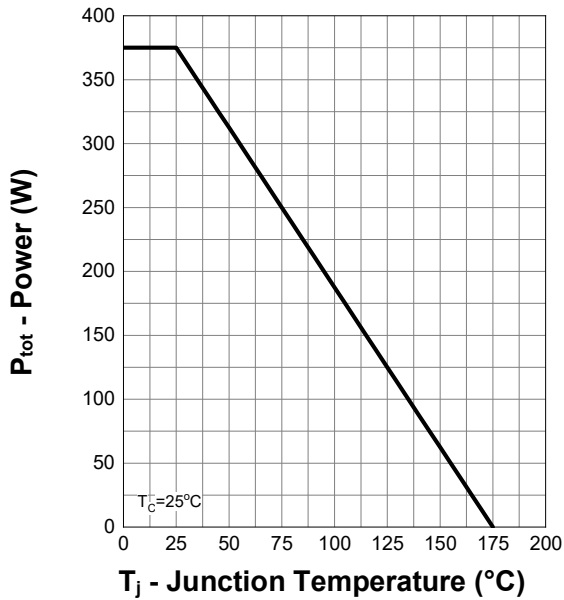
Electrical Characteristics ($T_A=25^\circ\text{C}$ Unless Otherwise Noted)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Static Characteristics						
BV_{DSS}	Drain-Source Breakdown Voltage	$V_{GS}=0\text{ V}$, $I_{DS}=250\ \mu\text{A}$	80	-	-	V
$V_{GS(th)}$	Gate Threshold Voltage	$V_{DS}=V_{GS}$, $I_{DS}=250\ \mu\text{A}$	2.0	-	4.0	V
I_{DSS}	Drain Leakage Current	$V_{DS}=64\text{ V}$, $V_{GS}=0\text{ V}$	-	-	1	μA
I_{GSS}	Gate Leakage Current	$V_{GS}=\pm 20\text{ V}$, $V_{DS}=0\text{ V}$	-	-	± 100	nA
$R_{DS(ON)}^a$	On-State Resistance	$V_{GS}=10\text{ V}$, $I_{DS}=50\text{ A}$	-	1.3	1.5	m Ω
		$V_{GS}=5\text{ V}$, $I_{DS}=30\text{ A}$	-	1.9	2.2	
Diode Characteristics						
V_{SD}^a	Diode Forward Voltage	$I_{SD}=50\text{ A}$, $V_{GS}=0\text{ V}$	-	-	1.3	V
t_{rr}	Reverse Recovery Time	$I_{SD}=50\text{ A}$, $V_{GS}=0\text{ V}$, $di_{SD}/dt=100\text{ A}/\mu\text{s}$	-	54	-	ns
Q_{rr}	Reverse Recovery Charge		-	78	-	nC
Dynamic Characteristics ^b						
C_{iss}	Input Capacitance	$V_{GS}=0\text{ V}$, $V_{DS}=40\text{ V}$, Frequency=1 MHz	-	7971	-	pF
C_{oss}	Output Capacitance		-	1112	-	
C_{rss}	Reverse Transfer Capacitance		-	53	-	
$t_{d(on)}$	Turn-on Delay Time	$V_{DS}=40\text{ V}$, $V_{GEN}=10\text{ V}$, $R_G=3.9\ \Omega$, $R_L=0.8\ \Omega$, $I_{DS}=50\text{ A}$	-	24	-	ns
t_r	Turn-on Rise Time		-	57	-	
$t_{d(off)}$	Turn-off Delay Time		-	94	-	
t_f	Turn-off Fall Time		-	56	-	
Gate Charge Characteristics ^b						
Q_g	Total Gate Charge	$V_{DS}=40\text{ V}$, $V_{GS}=10\text{ V}$, $I_{DS}=50\text{ A}$	-	141	-	nC
Q_{gs}	Gate-Source Charge		-	40	-	
Q_{gd}	Gate-Drain Charge		-	34	-	

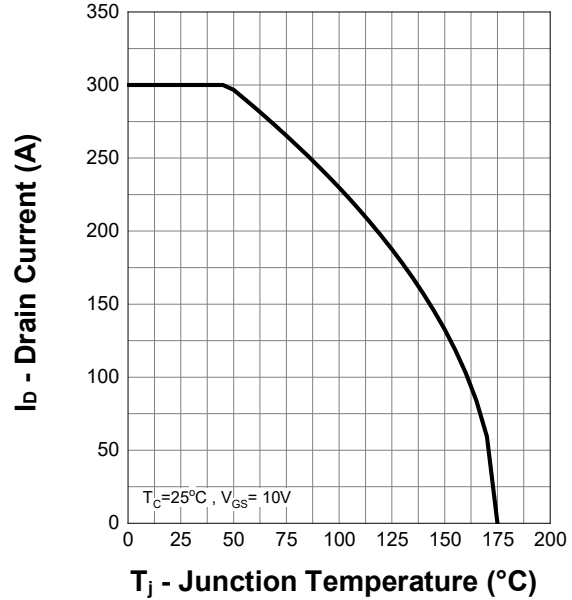
Notes:

- a. Pulse test; pulse width $\leq 300\ \mu\text{s}$, duty cycle $\leq 2\%$
 b. Guaranteed by design, not subject to production testing

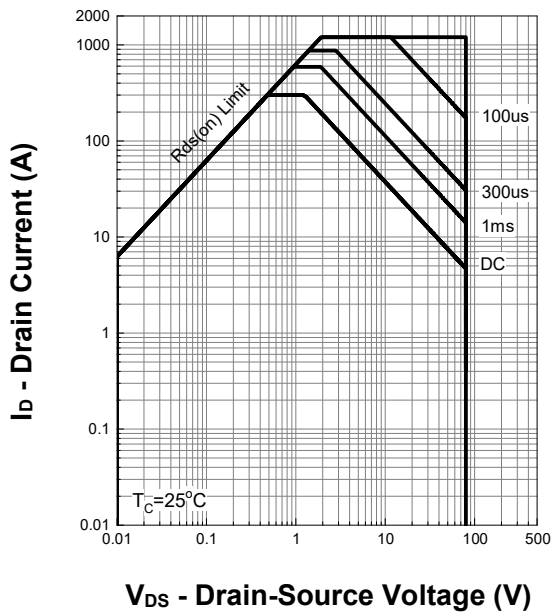
Power Capability



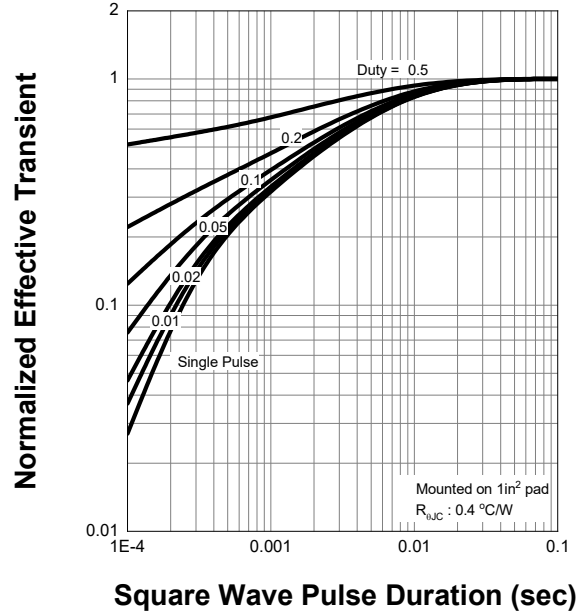
Current Capability



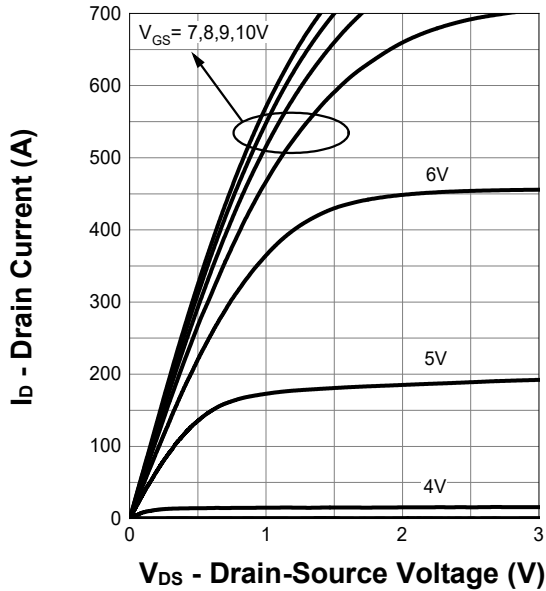
Safe Operating Area



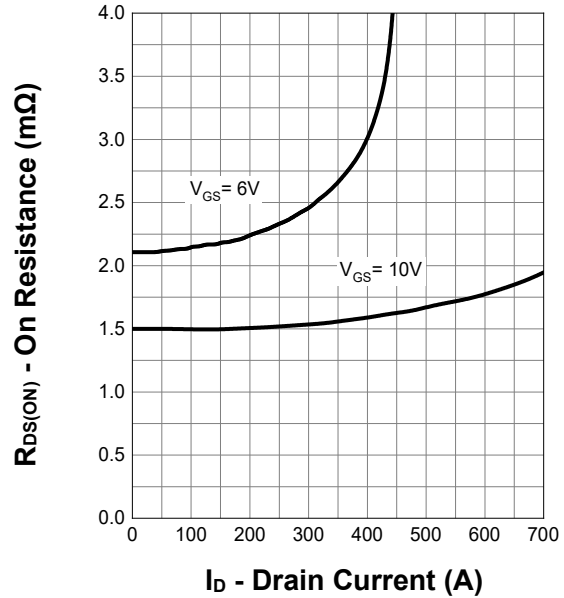
Transient Thermal Impedance



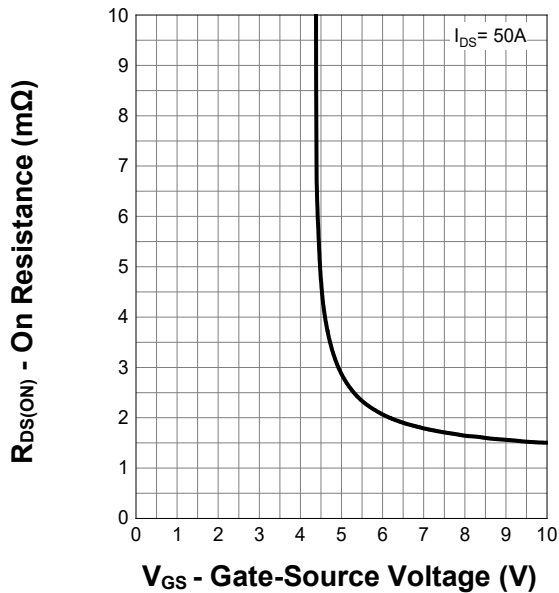
Output Characteristics



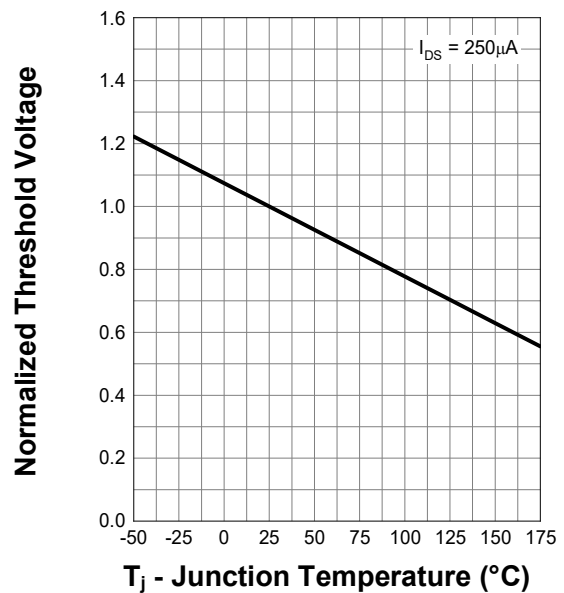
On Resistance



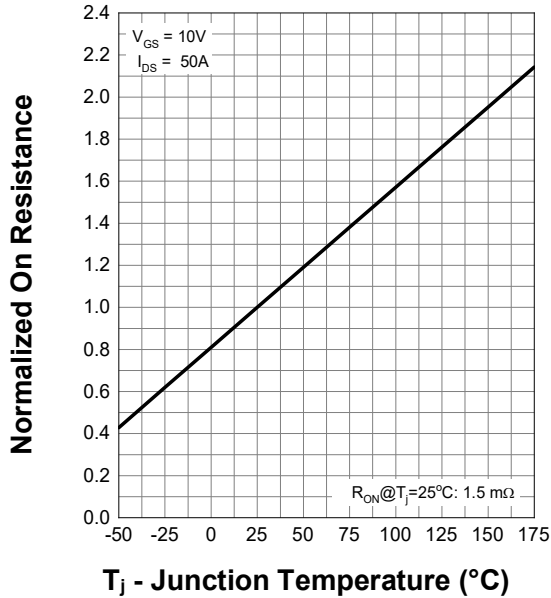
Transfer Characteristics



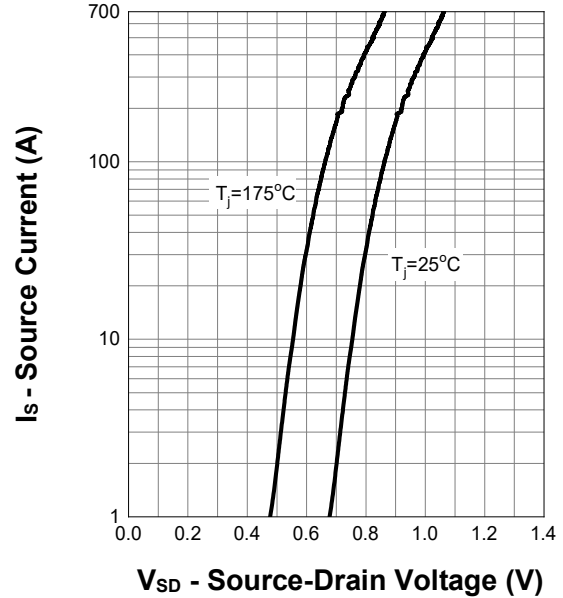
Normalized Threshold Voltage



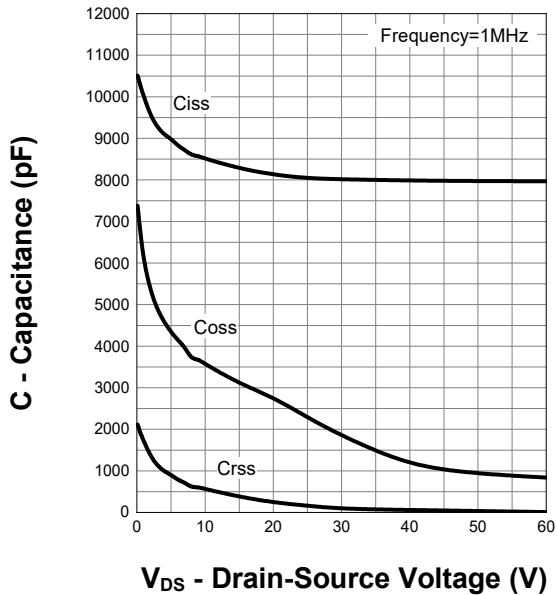
Normalized On Resistance



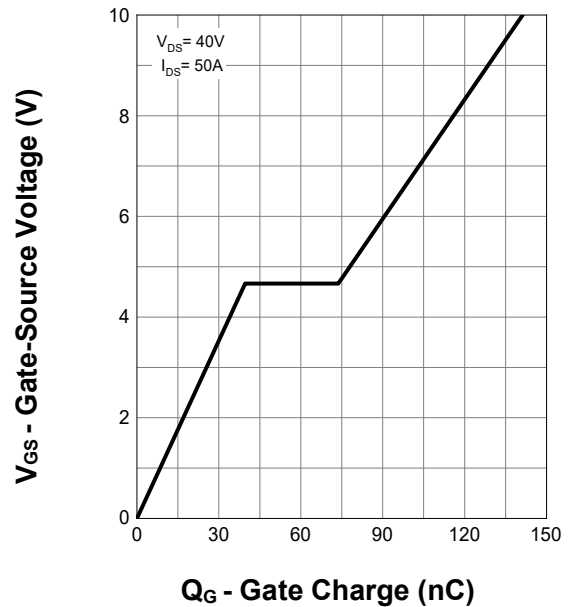
Diode Forward Current

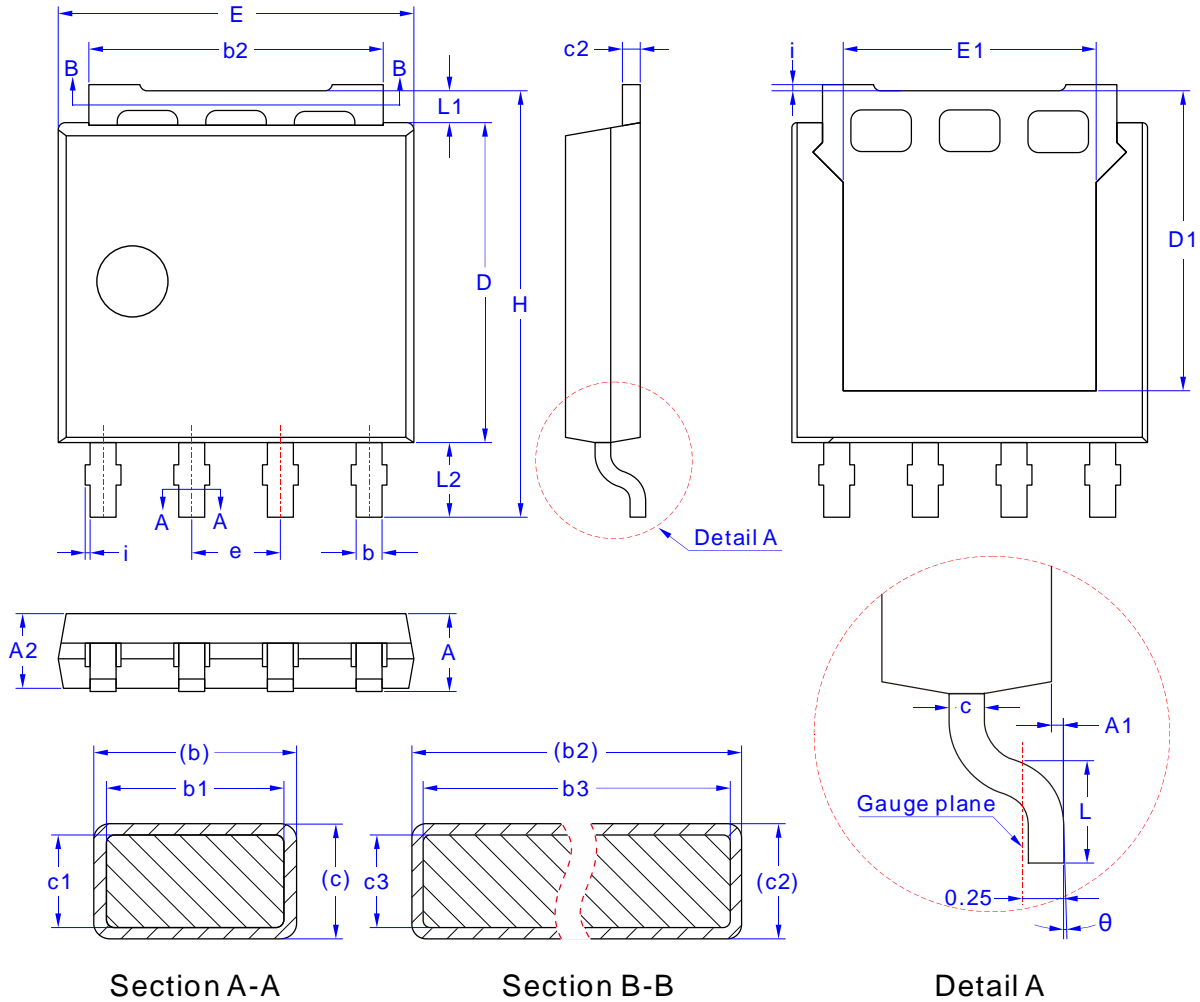


Capacitance



Gate Charge



LFPAK 5x6 Package


Symbol	Dimensions in Millimeters	
	MIN.	MAX.
A	1.00	1.30
A1	0	0.15
A2	0.98	1.12
b	0.35	0.50
b1	0.32	0.46
b2	4.02	4.41
b3	4.00	4.37
c	0.19	0.25
c1	0.17	0.23
c2	0.24	0.30
c3	0.22	0.28

Symbol	Dimensions in Millimeters	
	MIN.	MAX.
D	4.45	4.70
D1	-	4.45
E	4.95	5.30
E1	3.50	3.70
e	1.27 BSC	
H	5.95	6.25
i	-	0.25
L	0.40	0.85
L1	0.27	0.57
L2	0.80	1.30
θ	0°	8°

Flow (wave) soldering (solder dipping)

Product	Peak Temperature	Dipping Time
Pb device	245°C ±5°C	5sec±1sec
Pb-Free device	260°C +0/-5°C	5sec±1sec



This integrated circuit can be damaged by ESD. UniverChip Corporation recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedure can cause damage. ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

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