

## -200V P-Channel Enhancement Mode MOSFET

### Features

- Advanced HEFET™ Technology
- Ultra Low On-Resistance
- Excellent  $Q_g \times R_{DS(on)}$  Product
- 100% avalanche tested
- 175°C Operating Temperature
- Lead Free and Green Devices Available (RoHS Compliant)

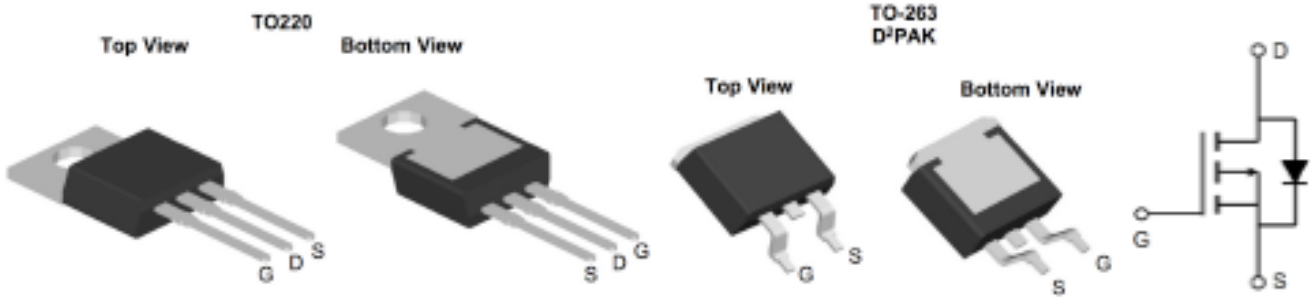
### Applications

- Motor Drives
- Uninterruptible Power Supplies
- DC/DC converter
- General Purpose Applications



$V_{DS} = -200V$   $I_D = -20A$

$R_{DS(ON)} < 260m\Omega$  @  $V_{GS} = 10V$



Product ID	Pack	Marking	Qty(PCS)
XPX20P20TU	TO-220-3L	XPX20P20TU XXX YYYY	1000
XPX20P20TU	TO-263-3L	XPX20P20TU XXX YYYY	800

### Absolute Maximum Ratings ( $T_C = 25^\circ C$ unless otherwise noted)

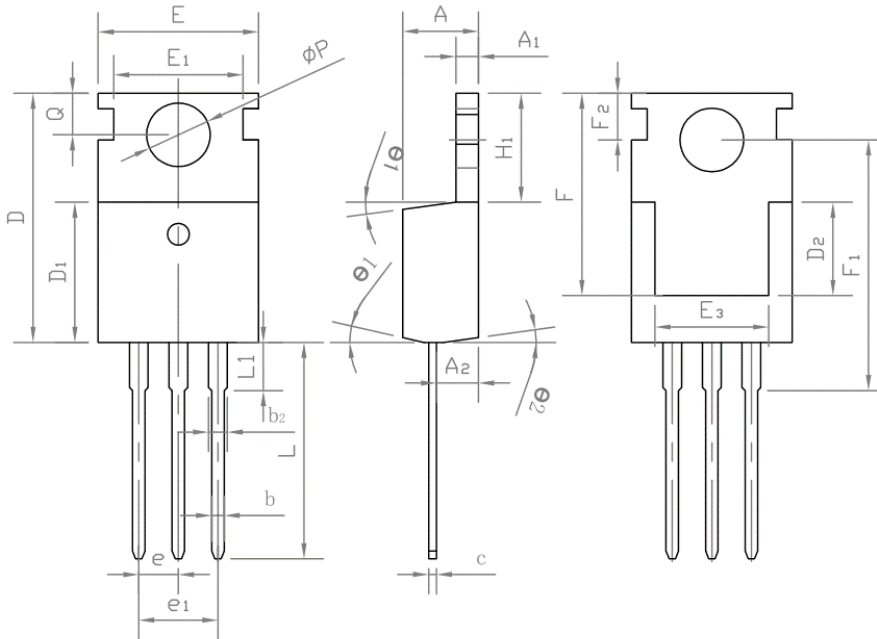
Symbol	Parameter	Rating	Units
V <sub>DS</sub>	Drain-Source Voltage	-200	V
V <sub>GS</sub>	Gate-Source Voltage	± 20	V
I <sub>D</sub> $T_C = 25^\circ C$	Continuous Drain Current	-20	A
I <sub>D</sub> $T_C = 100^\circ C$	Continuous Drain Current	-12	A
I <sub>DM</sub>	Pulsed Drain Current <sup>a</sup>	-65	A
E <sub>AS</sub>	Single Pulse Avalanche Energy <sup>b</sup>	1200	mJ
I <sub>AR</sub>	Repetitive Avalanche Current <sup>a</sup>	-15	A
P <sub>D</sub> $T_C = 25^\circ C$	Maximum Power Dissipation	325	W
T <sub>J</sub> , T <sub>stg</sub>	Operating Junction and Storage Temperature Range	-55 to +150	°C
R <sub>thJA</sub>	Maximum Junction-to-Ambient	62	°C/W
R <sub>thJC</sub>	Maximum Junction-to-Case (Drain)	1.0	°C/W

**-200V P-Channel Enhancement Mode MOSFET**
**Electrical Characteristics (T<sub>J</sub>=25°C, unless otherwise noted)**

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
V <sub>DS</sub>	Drain-Source Breakdown Voltage	V <sub>GS</sub> = 0 V, I <sub>D</sub> = -250 μA	-200	-254	-	V
V <sub>GS(th)</sub>	Gate-Source Threshold Voltage	V <sub>DS</sub> = V <sub>GS</sub> , I <sub>D</sub> = -250 μA	-2.0	3.5	-5.0	V
I <sub>GSS</sub>	Gate-Source Leakage	V <sub>GS</sub> = ± 20 V	-	-	± 100	nA
I <sub>DSS</sub>	Zero Gate Voltage Drain Current	V <sub>DS</sub> = -200 V, V <sub>GS</sub> = 0 V	-	-	100	μA
R <sub>DS(on)</sub>	Drain-Source On-State Resistance	V <sub>GS</sub> = -10 V, I <sub>D</sub> = -5.5 A	-	260	320	mΩ
g <sub>fs</sub>	Forward Transconductance	V <sub>DS</sub> = -50 V, I <sub>D</sub> = -6.6 A	4.1	-	-	S
C <sub>iss</sub>	Input Capacitance	V <sub>GS</sub> = 0 V, V <sub>DS</sub> = -25 V, f = 1.0 MHz,	-	2400	-	pF
C <sub>oss</sub>	Output Capacitance		-	740	-	pF
C <sub>rss</sub>	Reverse Transfer Capacitance		-	182	-	pF
Q <sub>g</sub>	Total Gate Charge	V <sub>GS</sub> = -10 V, I <sub>D</sub> = -18A, V <sub>DS</sub> = -160 V	-	-	88	nC
Q <sub>gs</sub>	Gate-Source Charge		-	-	14.1	nC
Q <sub>gd</sub>	Gate-Drain Charge		-	-	54	nC
t <sub>d(on)</sub>	Turn-On Delay Time	V <sub>DD</sub> = -100 V, I <sub>D</sub> = -18A R <sub>g</sub> = 9.1Ω,	-	28	-	ns
t <sub>r</sub>	Rise Time		-	86	-	ns
t <sub>d(off)</sub>	Turn-Off Delay Time		-	78	-	ns
t <sub>f</sub>	Fall Time		-	76	-	ns
R <sub>g</sub>	Gate Input Resistance	f = 1MHz, open drain	0.3	-	1.7	Ω
V <sub>SD</sub>	Body Diode Voltage	T <sub>J</sub> = 25 °C, I <sub>S</sub> = -18A, V <sub>GS</sub> = 0 V	-	-	-5	V
t <sub>rr</sub>	Body Diode Reverse Recovery Time	T <sub>J</sub> = 25 °C, I <sub>F</sub> = -18A, di/dt = 100 A/	-	500	600	ns
Q <sub>rr</sub>	Body Diode Reverse Recovery Charge		-	5.8	7.2	μC

**Note :**

- 1、 The data tested by surface mounted on a 1 inch<sup>2</sup> FR-4 board with 2OZ copper.
- 2、 The EAS data shows Max. rating . I<sub>AS</sub> = -18A, V<sub>DD</sub> = 50V, R<sub>G</sub> = 25Ω, Starting T<sub>J</sub> = 25 °C
- 3、 The test condition is Pulse Test: Pulse width ≤ 300μs, Duty Cycle ≤ 1%
- 4、 The power dissipation is limited by 150°C junction temperature
- 5、 The data is theoretically the same as I<sub>D</sub> and I<sub>DM</sub> , in real applications , should be limited by total power dissipation.

**Package Mechanical Data-TO-220-3L-SLK**


Symbol	Common		
	mm		
	Mim	Nom	Max
A	4.27	4.57	4.87
A1	1.15	1.30	1.45
A2	2.10	2.40	2.70
b	0.70	0.80	1.00
b2	1.17	1.27	1.50
D	0.40	0.50	0.65
D1	8.80	9.10	9.40
D2	5.70	6.70	7.00
E	9.70	10.00	10.30
E1	-	8.70	-
E2	9.63	10.00	10.35
E3	7.00	8.00	8.40
e		0.37	
e1		0.10	
H1	6.00	6.50	6.85
L	12.75	13.50	13.90
L1	-	3.10	3.40
Φp	3.45	3.60	3.75
Q	2.60	2.80	3.00
θ1	4°	7°	10°
θ2	0°	3°	6°
F	13.30	13.50	13.70
F1	15.50	15.90	16.30
F2	2.80	3.00	3.20

## -200V P-Channel Enhancement Mode MOSFET

Flow (wave) soldering (solder dipping)

Product	Peak Temperature	Dipping Time
Pb device	245°C ±5°C	5sec ±1 sec
Pb-Free device	260°C +0/-5°C	5sec ±1 sec



This integrated circuit can be damaged by ESD. UniverChip Corporation recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedure can cause damage. ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

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